NP

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/631,198	08/03/2000	Michael A. Lamson	TI-28674	9326

7590 05/03/2002

Gary C Honeycutt
Texas Instruments Incorporated
MS 3999
P O Box 655474
Dallas, TX 75265

EXAMINER	
NGUYEN, DILINH P	
ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 05/03/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/631,198	LAMSON ET AL.	
	Examiner	Art Unit	
	DiLinh Nguyen	2814	

-- The MAILING DATE of this communication appears on the cover she t with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 August 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) *23-29* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 1 recites the limitation "said metal layers" in line 9. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-15 and 17-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stearns et al. (U.S. Pat. 6,160,705) in view of Caletka et al. (U.S. Pat. 6104093).

- Regarding claims 1 and 14, Stearns et al. disclose a semiconductor device (figs. 1-3, column 3, lines 60 et seq.) comprising:

an insulating layer 14 having a first surface, a second surface and a plurality of vias (fig. 4, column 5, lines 40-50) filled with metal;

the first surface having one of the metal layers 16 attached to provide electrical ground potential of the ball grid array substrate (column 4, lines 47-51);

the second surface having the other of the metal layers 12 attached, portions thereof being configured as a plurality of electrical signal lines 22 (figs. 1-2 and 6-7,

column 5, lines 17 et seq.), further portions as a plurality of first electrical power line 24 and further potions as a plurality of second electrical power lines 26;

the signal lines being distributed relative to the first power lines and it would have been obvious that the inductive coupling between them reaches at least a minimum value, providing high mutual inductances and minimized effective self-inductance;

the signal lines further being electromagnetically coupled to the ground metal and it would have been obvious such that cross-talk between signal lines is minimized; and

an outermost insulating film 90 (column 5, lines 1-5 and column 9, lines 40-55) protecting the exposed surfaces of the power lines the film having a plurality of openings filled with metal suitable for contacting selected signal and power lines. It would have been obvious to form an outermost insulating film protecting the exposed surface of the ground layer, wherein the film having a plurality of openings filled with metal suitable for solder ball attachment.

Stearns et al. fail to disclose the designed for an IC flip-chip assembly. Caletka et al. disclose a semiconductor device comprising a designed for integrated circuit flip-chip assembly; wherein the IC chip 12 having an active surface including solder bumps (cover fig., column 4, lines 15 et seq.); and a plurality of solder balls attached under the surface of a PCB 16 for outside word connection. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Stearns et al. to provide a designed for IC flip-chip assembly so that with ordinary to expand the applicability of the semiconductor device.

- Regarding claims 2 and 4-7, it is conventional in the art to find the number of the I/O's ranges, a width of the signal lines and power lines through routine and obvious experimentation. It would have been obvious to one having ordinary skill to find the ranges of I/O, a width of the signal lines and power lines since it is desirable to form devices that are structurally and electrically sound.
- Regarding claim 3, Stearns et al. disclose the thickness of the substrate may be provided in various thickness (column 3, lines 60-63).
- Regarding claim 8, Stearns et al. disclose the metal layers 12 and 16 may be provided as virtually any conductive metal layer suitable, preferably copper layer with nickel and gold plating provided at connections as needed (column 4, lines 5-12).
- Regarding claim 9, Stearns et al. disclose the dielectric layer 14 may be fabricated using virtually any dielectric or insulator material such as a thin film or polyimide or an organic resin based glass fiber reinforced dielectric laminate (column 4, lines 12-15).
- Regarding claim 10, Stearns et al. disclose the vias are filled with electrically conductive material (column 5, lines 40-54).
- Regarding claim 11, it would have been obvious to one having ordinary skill in the art at the time the inventions was made to provide the second power lines are structured as distributed areas having wide geometries for minimizing self-inductance and merging into a central area supporting the chip.

- Regarding claim 12, Stearns et al. disclose the outermost insulating films 90 are the solder mask layers (column 5, lines 1-5 and column 9, lines 40-55).
- Regarding claim 13, Stearns et al. disclose the solder balls are typically composed of eutectic Sn63/Pb37 or similar compositions (column 5, lines 32-37).
- Regarding claim 15, Caletka et al. disclose an underfill material 17 filling any gaps between the chip and the substrate.
- Regarding claims 17-18, Caletka et al. disclose a body 26 surrounding the chip, wherein the body 26 is selected from a group consisting of epoxy based molding compounds suitable for adhesion to the chip (column 4, lines 55-65).
- Regarding claim 19, Caletka et al. disclose a heat sink 22 positioned on the outer surface of the body 26 (cover fig., column 4, lines 22-25).
- Regarding claims 20-21, Caletka et al. disclose the plurality of solder balls 14.
- Regarding claim 22, it would have been obvious to provide the thickness of the package is in the range from about 250-800 μm, excluding the thickness of the heat sink, the design alternative.

5. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stearns et al. (U.S. Pat. 6,160,705) in view of Caletka et al. (U.S. Pat. 6104093) and further in view of Thomas (U.S. Pat. 6228680).

Stearns et al. and Caletka et al. disclose the claimed invention except for the underfill material is a polymeric precursor. Thomas discloses a semiconductor device (cover fig.) comprising: a polymeric precursor 18 made of an epoxy base material filled with silica and anhydrides (column 7, lines 64 et seq. and column 11, lines 26-35)

requiring thermal energy for curing to form a polymeric encapsulant. Therefore, it would have been obvious to one having ordinary skill in the art to modify the devices of Stearns et al. and Caletka et al. to provide a low stress in the dielectric layers of the chip and in the solder balls for operating the semiconductor assembly as shown by Thomas.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DiLinh Nguyen whose telephone number is (703) 305-6983. The examiner can normally be reached on 8:00AM - 6:00PM (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, OLIK CHAUDHURI can be reached on (703) 308-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

DLN
April 25, 2002

OLIK CHAUDHURI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800